Hall Ticket No: | | | | | | | | | | |

Question Paper Code: 24VESP101

MADANAPALLE INSTITUTE OF TECHNOLOGY & SCIENCE, MADANAPALLE

(UGC-AUTONOMOUS)

M.Tech. I Year I Semester (R24) Regular End Semester Examinations, March - 2025

CMOS DIGITAL IC DESIGN

(M.Tech. – VLSI Design and Embedded Systems)

Time: 3Hrs **Max Marks: 60**

Attempt all the questions. All parts of the question must be answered in one place only.
In Q.No 1 to 5 answer either A or B only

Q.No	Question	Marks	CO	BL
Q.1(A)	Compare CMOS Inverter and Pseudo NMOS inverter; list the drawbacks of Pseudo NMOS Logic over CMOS logic.	12M	1	2
	OR			
Q.1(B)	Explain the voltage transfer characteristics of a CMOS inverter with a neat diagram.	12M	1	2
Q.2(A)	Design one-bit full adder using CMOS logic and explain its working.	12M	2	3
	OR			
Q.2(B)	Implement the 2-input universal gates using transmission gate logic.	12M	2	3
Q.3(A)	Draw the logic diagram of a CMOS clocked SR flip-flop and explain with the help of a truth table.	12M	3	3
	OR			
Q.3(B)	Explain about the Behavior of bistable elements.	12M	3	2
Q.4(A)	Discuss about High performance Dynamic CMOS circuits.	12M	4	2
	OR			
Q.4(B)	Explain voltage bootstrapping with an example.	12M	4	2
Q.5(A)	Compare the performance of SRAM and DRAM. Draw the SRAM cell and explain its Read and Write operation.	12M	5	2
	OR			
Q.5(B)	Mention different types of RAM cells. Draw and explain the operation of a single bit dynamic RAM cell.	12M	5	2

***** END*****

Hall Ticket No: | | | | | | | | | | | Question Paper Code: 24VESP102

MADANAPALLE INSTITUTE OF TECHNOLOGY & SCIENCE, MADANAPALLE

(UGC-AUTONOMOUS)

M.Tech I Year I Semester (R24) Regular End Semester Examinations, March - 2024

MICROCONTROLLERS AND PROGRAMMABLE DIGITAL SIGNAL PROCESSORS

(M.Tech. – VLSI Design and Embedded Systems)

Time: 3Hrs **Max Marks: 60**

Attempt all the questions. All parts of the question must be answered in one place only.
In Q.No 1 to 5 answer either A or B only

Q.No	Question	Marks	CO	BL
Q.1(A)	i) Implement a simple bit-band operation to toggle an LED using an ARM-based microcontroller.	6M	1	3
	ii) What are the different operation modes of an ARM processor?	6M	1	2
	OR			
Q.1(B)	i) Illustrate the role of registers in the ARM programming model.	6M	1	2
	ii) Write a C program to toggle an LED for 5 sec using an ARM-based microcontroller.	6M	1	3
Q.2(A)	i) What is the function of the Nested Vectored Interrupt Controller (NVIC) in ARM processors?	6M	2	2
	ii) Describe the process of interrupt sequence from occurrence to execution.	6M	2	2
	OR			
Q.2(B)	i) Write a program to configure a GPIO pin as an output and toggle it every 5 second using a timer.	6M	2	2
	ii) What are fault exceptions, and how do they differ from other types of exceptions?	6M	2	3
Q.3(A)	i) What are the key features of the GPIO module in the LPC17xx microcontroller?	6M	3	2
	ii) Implement a LPC17xx timer interrupt to generate a periodic delay of 2 second.	6M	2	3
	OR			
Q.3(B)	i) Describe the different timer modes available in LPC17xx.	6M	3	3
	ii) Configure a PWM channel on LPC17xx to generate a signal with a 75% duty cycle.	6M	3	3
Q.4(A)	i) What are the key features of the TI DSP processor family?	6M	4	2
	ii) Implement a simple FIR filter using a TI DSP processor.	6M	4	2
	OR			
Q.4(B)	i) Describe the function of the MAC (Multiply-Accumulate) unit in DSP processors.	6M	4	2
	ii) What are the advantages of using a DSP processor over a general-purpose microcontroller?	6M	4	2
Q.5(A)	i) Describe the **instruction set and memory architecture** of the **TMS320C55x series**.	6M	5	2
	ii) What are the advantages of using **TMS320C6000 series DSP processors** in real-time signal processing applications?	6M	5	2
	OR			
Q.5(B)	i) What are the different types of **assembly instructions** in the **TMS320C6000 family**, and how are they categorized?	6M	5	2
	ii) What are the key differences between the **TMS320C6000 and TMS320C55x architectures**?	6M	5	2

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Hall Ticket No: | | | | | | | | | | |

Question Paper Code: 24VESP403

MADANAPALLE INSTITUTE OF TECHNOLOGY & SCIENCE, MADANAPALLE

(UGC-AUTONOMOUS)

M.Tech I Year I Semester (R24) Regular End Semester Examinations, March - 2025

FPGA ARCHITECTURES AND APPLICATIONS

(M.Tech. – VLSI Design and Embedded Systems)

Time: 3Hrs **Max Marks: 60**

Attempt all the questions. All parts of the question must be answered in one place only.
In Q.No 1 to 5 answer either A or B only

Q.No	Question	Marks	CO	BL
Q.1(A)	A combinational circuit is defined as follows: F1= AB'C'+ AB'C + ABC and F2 =A'BC+ AB'C+ ABC implement using ROM, PAL and PLA.	12M	1	3
	OR			
Q.1(B)	(i) Distinguish between ROM, PLA and PAL. (ii) Draw and explain the general block diagram of CPLD.	12M	1	3
Q.2(A)	(i) Explain about programmable interconnects in FPGAs. (ii) With examples, explain about look up tables in FPGA.	12M	2	2
	OR			
Q.2(B)	(i) Distinguish between Anti-fuse technology and SRAM technology. (ii) Write short note on applications of FPGAs.	12M	2	2
Q.3(A)	(i) With block diagram, explain about CLB block in Xilinx 3000 series. (ii) Explain about dedicated specialized components of FPGAs.	12M	3	2
	OR			
Q.3(B)	(i) With block diagram, explain about CLB block in Xilinx 3000 series. (ii) Write a brief note on Static-RAM implementation of FPGA technology.	12M	3	3
Q.4(A)	(i) Explain the features of anti-fuse programmed FPGAs. (ii) Explain how Actel ACT-1 logic module acts as a boolean function generator.	12M	4	3
	OR			
Q.4(B)	(i) Explain about Actel ACT-1 programmable interconnect architecture. (ii) Illustrate the routing architecture of an Actel ACT FPGA.	12M	4	3
Q.5(A)	(i) Realize 3-bit full adder using Actel FPGAs. (ii) Design and explain about a fast DMA controller in detail.	12M	5	4
	OR			
Q.5(B)	(i) Design and explain about a fast video controller. (ii) Design position tracker of a robot manipulator with help of FPGAs.	12M	5	4

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Hall Ticket No: | | | | | | | | | | |

Question Paper Code: 24VESP404

MADANAPALLE INSTITUTE OF TECHNOLOGY & SCIENCE, MADANAPALLE

(UGC-AUTONOMOUS)

M.Tech I Year I Semester (R24) Regular End Semester Examinations, March - 2025

LOW POWER VLSI DESIGN

(M.Tech. – VLSI Design and Embedded Systems)

Time: 3Hrs **Max Marks: 60**

Attempt all the questions. All parts of the question must be answered in one place only.
In Q.No 1 to 5 answer either A or B only

Q.No	Question	Marks	CO	BL
Q.1(A)	i) Discuss the importance of low power VLSI design at advance technology nodes.	6M	1	2
	ii) Explain about switching power dissipation in CMOS digital circuits?	6M	1	2
	OR			
Q.1(B)	i) Explain the concept of Glitch power dissipation in detail.	6M	1	2
	ii) Write short noes on (a) DIBL (b) Punch Through.	6M	1	2
Q.2(A)	Demonstrate the MTCMOS and VTCMOS circuits for leakage power reduction with neat sketches.	12M	2	3
	OR			
Q.2(B)	Illustrate how pipelining and parallel processing approaches can be utilized for low power design with suitable examples.	12M	2	3
Q.3(A)	Realize Half adder circuit with static CMOS Logic.	12M	3	4
	OR			
Q.3(B)	Explain the basic theory, operation and performance evaluation of carry look-ahead adders.	12M	3	4
Q.4(A)	Construct the Baugh Wooley multiplier and explain its operation, also write its algorithm.	12M	4	4
	OR			
Q.4(B)	i) Discuss types of multiplier architectures.	6M	4	4
	ii) Draw a flowchart or state diagram illustrating the steps involved in Booth's multiplication. Give an example.	6M	4	4
Q.5(A)	i) Draw and explain the Pre-charge and Equalization Circuit used in memories.	6M	5	4
	ii) Explain the operation of SRAM and explain Read and Write access transistor operation with neat diagram.	6M	5	4
	OR			
Q.5(B)	i) Explain the read and write operations for a one-transistor transistor DRAM cell.	6M	5	4
	ii) Explain the difference between SRAM and DRAM?	6M	5	4

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Hall Ticket No: | | | | | | | | | | |

Question Paper Code: 24RMP101

MADANAPALLE INSTITUTE OF TECHNOLOGY & SCIENCE, MADANAPALLE

(UGC-AUTONOMOUS)

M.Tech I Year I Semester (R24) Regular End Semester Examinations, March - 2025

RESEARCH METHODOLOGY AND IPR

(Common to VLSI and CSE)

Time: 3Hrs **Max Marks: 60**

Attempt all the questions. All parts of the question must be answered in one place only.
In Q.No 1 to 5 answer either A or B only

Q.No	Question	Marks	CO	BL
Q.1(A)	Explain the different types of research and their significance in problem formulation. Discuss the role of a literature review in identifying the research gap.	12M	1	2
	OR			
Q.1(B)	Explain the objectives and types of research. Describe the research process and different research approaches. Discuss the importance of a literature review, including information sources, retrieval tools, indexing services, and citation indexes. How can a research gap be identified and hypothesized.	12M	1	2
Q.2(A)	Define and explain the different types of experimental designs used in research. Elaborate on each type with suitable examples, highlighting their significance, strengths, and limitation	12M	2	2
	OR			
Q.2(B)	Compare between Primary Data and Secondary Data with appropriate examples. Additionally, explain the classification of data with relevant illustrations.	12M	2	2
Q.3(A)	Interpret the Mean, Median, Mode, Range, and Standard Deviation for the given dataset: {2, 5, 7, 6, 4, 8}. Show all necessary steps and calculations.	12M	3	2
	OR			
Q.3(B)	Explain the term plagiarism, and why is it a serious concern in academic and research writing? Discuss various online tools used for detecting plagiarism. As a researcher, what precautions should be taken to ensure the publication of a plagiarism-free report.	12M	3	2
Q.4(A)	Explain the importance of intellectual property rights. Explain the role of WTO in promoting IPR.	12M	4	2
	OR			
Q.4(B)	Explain the following intellectual property rights (IPRs) in brief, highlighting their significance and key features: (a) Patents (b) Designs (c) Trademarks (d) Copyright	12M	4	2
Q.5(A)	List and identity the categories of inventions that are non-patentable and write a short note on that. Provide examples to justify why these inventions do not qualify for patent protection.	12M	5	3
	OR			
Q.5(B)	An entrepreneur has developed an innovative wearable health tracker. Apply your understanding of patents to explain the filing process. Discuss the advantages of patent protection and analyze the role of licensing in business growth and international expansion.	12M	5	3

***** END*****